ABSTRACT

MULTIPHASE RETIMING MECHANISM

A system and method for reducing timing uncertainties in a serial data signal. A system may comprise a transmitter configured to transmit serial data to a receiver through a transmission medium. The receiver may comprise a retiming mechanism configured to sample the serial data using a particular phase of a clock at a point in time when the serial data signal may not be likely to experience jitter. The retiming mechanism may comprise a plurality of first units, e.g., flip-flops, where each of the first units is configured to sample the serial data using a particular phase of the clock. Each of the first units may be connected to a particular second unit, e.g., transmission gate. Each of the second units may be configured to output the value of the serial data sampled by the associated first unit upon activation. The data outputted may subsequently become part of the retimed data.